Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SAILESH CHITTIPEDDI AND ARUN K. NANDA

Appeal No. 1997-3734
Application No. 08/329,806

ON BRIEF

Before JOHN D. SMITH, HAIRSTON, and TIMM, *Administrative Patent Judges*.

TIMM, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1-9, which are all of the claims pending in this application.

BACKGROUND

Appellants' invention relates to a method of integrated circuit fabrication which involves the use of tungsten conductors (Specification, page 1, lines 3-5). Claim 1 is illustrative:

1. A method of semiconductor integrated circuit fabrication comprising:

forming a dielectric upon a substrate;

forming an opening in said dielectric, exposing said substrate;

forming a layer of material chosen from the group consisting of polysilicon and amorphous silicon within said opening, and overlying all of the exposed portion of said substrate and said dielectric, said layer not completely filling said opening;

exposing said layer of material to WF_6, thereby forming a tungsten plug which completely fills said opening, and forming a tungsten layer which covers said dielectric;

etching said tungsten layer.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Shioya et al. (Shioya)	4,906,593	Mar. 06, 1990
Dixit et al. (Dixit)	4,960,732	Oct. 02, 1990
Sun et al. (Sun)	4,994,410	Feb. 19, 1991
Chung et al. (Chung)	5,094,981	Mar. 10, 1992
Manocha et al. (Manocha)	5,141,897	Aug. 25, 1992
Japanese Patent Applications		
Fujita	62-243325	Oct. 23, 1987
Shiki (Tadaki)[1]	63-052441	Mar. 05, 1988
Kobayashi et al. (Kobayashi)	2-090518	Mar. 30, 1990

2 Wolf, *Silicon Processing for the VLSI Era* 240-254 (1990).

[1] As both the Examiner and the Appellants use "Tadaki" to refer to this reference we will do likewise.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tadaki, Fujita, Kobayashi, Shioya and Wolf taken together. Claims 3-7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tadaki, Fujita, Kobayashi, Shioya and Wolf taken together and further in view of Sun, Chung, Dixit, and Kobayashi. Claims 8 and 9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tadaki, Fujita, Kobayashi, Shioya and Wolf taken together and further in view of Dixit, Manocha, and Tadaki. We reverse substantially for the reasons presented in the Brief and add the following primarily for emphasis.

OPINION

"A critical step in analyzing the patentability of claims pursuant to section 103(a) is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field." *In re Kotzab*, 217 F.3d 1365, 1369-70, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 2000). "The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time." *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)(quoting *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985). To establish a *prima facie* case of obviousness, "there must be some teaching, suggestion or motivation in the prior art to make the specific combination that was made by the applicant." *In re Dance*, 160 F.3d 1339, 1343, 48

USPQ2d 1635, 1637 (Fed. Cir. 1998). "In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1458 (Fed.Cir. 1998).

Focusing on claim 1, the only independent claim, we note that this claim requires the formation of a layer of polysilicon or amorphous silicon overlying all of the exposed portion of the substrate and dielectric. This layer of silicon material is then exposed to WF_6 to form a tungsten layer which *covers* said dielectric. It is this tungsten layer *covering* the dielectric which is etched. In the processes of Tadaki, Fujita, Kobayashi[2], and Shioya, the silicon layer is etched back before any step of converting silicon to tungsten. None of these references describe etching a tungsten layer much less a tungsten layer covering the dielectric. To remedy this deficiency, the Examiner looks to the disclosure in Wolf at page 245 which summarizes two methods for the implementation of vertical vias. In describing one of these methods, Wolf states the following:

> 1. *Filling of vias through deposition of metal into the opened via to form a plug in the opening*. In theory, this can be accomplished either independently of the metal-runner formation process, or through simultaneous fabrication of the plugs and metal runner. An example of the latter is the deposition and patterning of a blanket CVD W layer.

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[2] In making our determination, we rely on the translations of the Japanese documents which are of record in the application.

Turning to page 246 of Wolf, we note that silicon reduction in which WF_6 reacts with solid silicon to form tungsten (W) is described as a process of selectively depositing W (p. 246, lines 29-31). On pages 247 and 248, Wolf describes the blanket CVD W and etchback process as a process involving hydrogen or silane gas reduction of WF_6. Therefore, Wolf suggests etching a CVD W layer deposited by hydrogen or silane gas reduction to form plugs and runners simultaneously. Wolf does not describe using a process of silicon reduction to form plugs and runners simultaneously. Looking at the prior art as a whole, we cannot say that it would have been obvious to one of ordinary skill in the art to eliminate the step of etching the silicon material of any of the Tadaki, Fujita, Kobayashi or Shioya processes, convert a silicon layer covering the dielectric to tungsten and then etch the tungsten. There is simply no reason, suggestion, or motivation in the prior art, as applied by the Examiner, to perform the process in the claimed sequence.

While, after knowing the direction in which the inventor proceeded, the invention may seem like a logical step forward, it cannot be said to have been obvious based solely on the information known prior to the invention. We conclude that the Examiner has not established a *prima facie* case of obviousness with respect to the subject matter of claims.

CONCLUSION

To summarize, the decision of the Examiner to reject claims 1-9 under 35 U.S.C. § 103 is reversed.

REVERSED

JOHN D. SMITH	)
Administrative Patent Judge	)
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	)
	) BOARD OF PATENT
KENNETH W. HAIRSTON	) APPEALS
Administrative Patent Judge	) AND
	) INTERFERENCES
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CATHERINE TIMM	)
Administrative Patent Judge	)

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